# TDLM025100

## Document Category: Product Specification

***RF Power Limiter, 10 MHz–2.5 GHz***

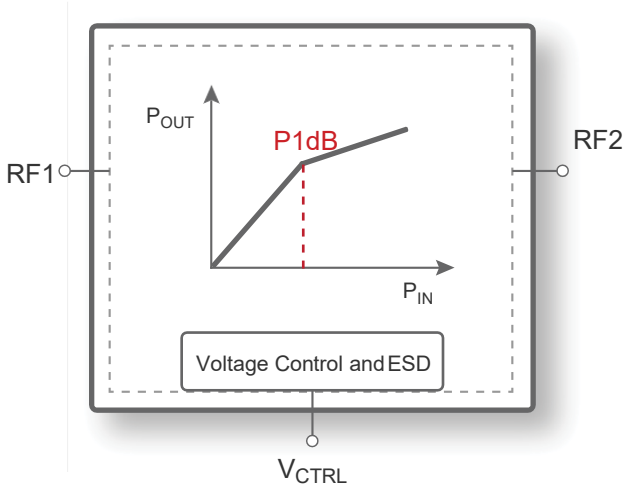
## Features

- Monolithic drop-in solution with no external bias components
- Adjustable low power limiting threshold from +7 dBm to +13 dBm
- High maximum power handling of 50 dBm, 100 W pulsed
- Positive threshold control from +0V to +0.3V
- Fast response time of less than 1 ns
- Packaging – 24-pad 4 × 4 × 0.85 mm CLGA
- Qualified for use in harsh environments

## Applications

- Satellite transceivers and antennas
- Sensitive orbital T/R Modules

**Figure 1 • *TDLM025100 Functional Diagram***




## Product Description

The TDLM025100 is a RF power limiter qualified for operating in harsh environments, including military, space , avionics and medical applications.

Unlike traditional PIN diode solutions, the TDLM025100 achieves an adjustable input 1 dB compression point or limiting threshold via a low current control voltage ($V_{CTRL}$), eliminating the need for external bias components such as dc blocking capacitors, RF choke inductors and bias resistors.

It delivers low insertion loss and high linearity under non-limiting power levels and extremely fast response time in a limiting event, ensuring protection of sensitive circuitry. It also offers excellent ESD rating and ESD protection.

The TDLM025100 is a monolithic solution manufactured on a ruggedized process offering the performance of GaAs with the economy and integration of conventional CMOS.

# Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

## ESD Precautions

When handling this UltraCMOS® device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

## Latch-up Immunity

The TDLM025100 is immune to single event induced latch-up.

**Table 1 • *Absolute Maximum Ratings for TDLM025100***

| Parameter/Condition | Min | Max | Unit |
|---|---|---|---|
| Control voltage, $V_{CTRL}$<br>Power limiting mode | 0 | 3.6 | V |
| RF input power, Pulsed[1] | | 50 | dBm |
| Storage temperature range | –65 | +150 | °C |
| ESD voltage HBM, all pins[2] | | 7000 | V |
| ESD voltage CDM, all pins[3] | | 2000 | V |

**Notes:**
1) Pulsed, 1.0% duty cycle of 10 µs pulse width in 1 ms period, 50 Ω at +25 °C.
2) Human body model (MIL-STD 883 Method 3015).
3) Charged device model (JEDEC JESD22-C101).

## Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the TDLM025100. Devices should not be operated outside the operating conditions listed below.

**Table 2 • *Recommended Operating Conditions for TDLM025100***

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Control voltage, $V_{CTRL}$ | | | | |
| Power limiting mode | 0 | | +0.3 | V |
| Power reflecting mode | 0 | | +3.0 | V |
| RF input power, CW(*) | | | Fig. 2 | dBm |
| Operating ambient temperature range - $T_{ambient}$ | –55 | +25 | +105 | °C |
| Operating max junction temperature | | | +150 | °C |

**Note:** * See Fig. 2.

## Electrical Specifications

**Table 3** provides the TDLM025100 key electrical specifications at +25 °C ($Z_S$ = $Z_L$ = 50 Ω), unless otherwise specified.

**Table 3 • *TDLM025100 Electrical Specifications***

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operation frequency* | | 10 MHz | | 2.5 GHz | As shown |
| **Power limiting mode** | | | | | |
| Insertion loss | 1 GHz, VCTRL = 0V, Ta = -55 °C to +85 °C, Typ value is +25 °C<br>2 GHz, VCTRL = 0V, Ta = -55 °C to +85 °C, Typ value is +25 °C<br>2.5 GHz, VCTRL = 0V, Ta = -55 °C to +85 °C, Typ value is +25 °C | | 0.30<br>0.40<br>0.45 | 0.60<br>0.60<br>0.60 | dB<br>dB<br>dB |
| Return loss | 10 MHz–3 GHz, $V_{CTRL}$ = 0V<br>3–6 GHz, $V_{CTRL}$ = 0V | | 22<br>12 | | dB<br>dB |
| Gain Compression with +13dBm Input Power | $V_{CTRL}$ = 0V @ 1 GHz, 2 GHz, and 2.5 GHz<br>Ta = -55 °C to +85 °C | | 0.85 | 1.25 | dB |
| Leakage power(1) | $V_{CTRL}$ = 0V, @ 1 GHz, 2 GHz, and 2.5 GHz<br>Ta = -55 °C to +85 °C | | 15.8 | 16.9 | dBm |
| Input IP2 | $V_{CTRL}$ = 0V @ 915 MHz<br>$V_{CTRL}$ = 0V @ 6 GHz | | 88<br>70 | | dBm<br>dBm |
| Input IP3 | $V_{CTRL}$ = 0V @ 915 MHz<br>$V_{CTRL}$ = 0V @ 6 GHz | | 37<br>31 | | dBm<br>dBm |
| Response time | 1 GHz | | 0.6 | | ns |
| Recovery time(4) | 1 GHz, $P_{IN}$, Pulse = 30 dBm | | 1.0 | | ns |
| **Power reflecting mode(2)** | | | | | |
| Leakage power(1) | $V_{CTRL}$ = +3.0V @ 915 MHz | | –41 | | dBm |
| Switching time(3) | State change to 10% RF | | 2.7 | | µs |

**Notes:**

1) Measured with +30 dBm CW applied at input.
2) This mode requires the control voltage to toggle between +3.0V and 0V. At +3.0V, the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source.
3) State change is $V_{CTRL}$ toggle from 0V to +3.0V.
4) Pulsed, 1% duty cycle of 10 µs pulse width in 1 ms period, 50 Ω @ +25 °C.

## Thermal Data

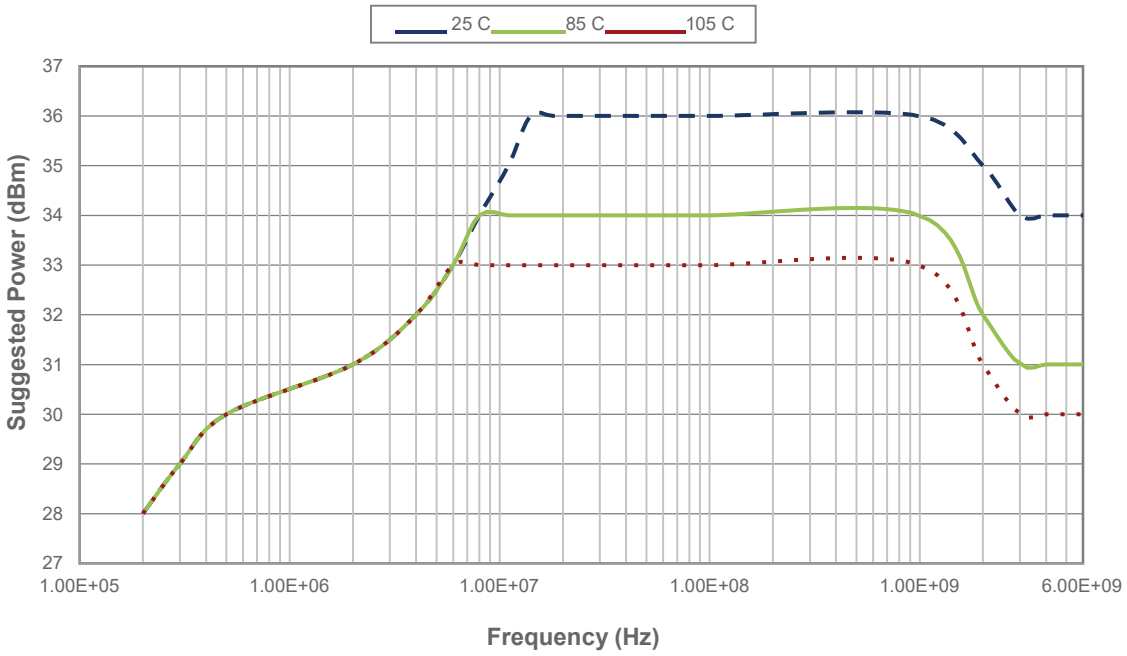
Table 4 • *Thermal Data for TDLM025100*

| Parameter | Typ | Unit |
|---|---|---|
| $\Theta_{JC}$, junction-to-case thermal resistance | 25 | °C/W |

## Power De-rating Curve

Figure 2 shows the power de-rating curve indicating maximum allowable operating RF input power (CW) up to the part's maximum operating ambient temperature of +105 °C. This RF input power maintains the maximum operating junction temperature requirement of +150 °C.

Figure 2 • *Power De-rating Curve, 10 MHz–6 GHz, +25 °C to +105 °C Ambient, CW, 50 Ω*(*)




Note: * High frequency CW power handling can be improved with 0.30 pF capacitive matching on input and output RF ports.

## Dual Mode Operation

### *Power Limiting Mode*

The TDLM025100 performs as a linear power limiter with adjustable P1dB/limiting threshold. The P1dB/ limiting threshold can be adjusted by changing the control voltage between 0V and +0.3V. If unbiased, or if $V_{CTRL}$ = 0V, the TDLM025100 still offers power limiting protection.

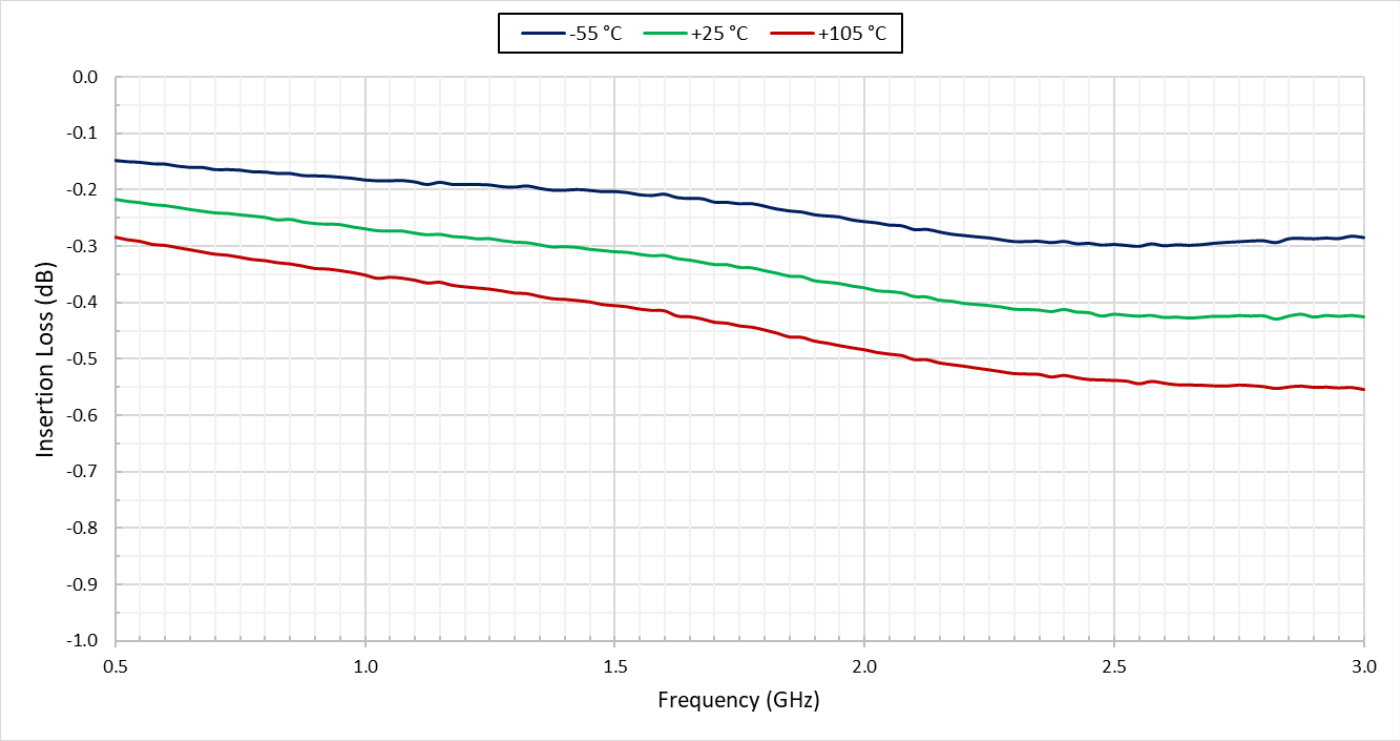
### *Power Reflecting Mode*

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +3.0V and 0V based on the system protection requirements. At +3.0V, the limiter impedance to ground is less than 1 Ω and most of the incident power will be reflected back to the source. At 0V, the device operates as in power limiting mode.

## Typical Performance Data

**Fig. 3–Figure 16** show the typical performance data at +25 °C ($Z_S$ = $Z_L$ = 50 Ω), unless otherwise specified.

**Figure 3 • *Insertion Loss vs Temp (Soldered 24L CLGA Package)***




***Note:*** Figures 4-17 were taken using a 12L, 3x3 mm Plastic QFN Package

**Figure 4 • *Input Return Loss vs Temp***

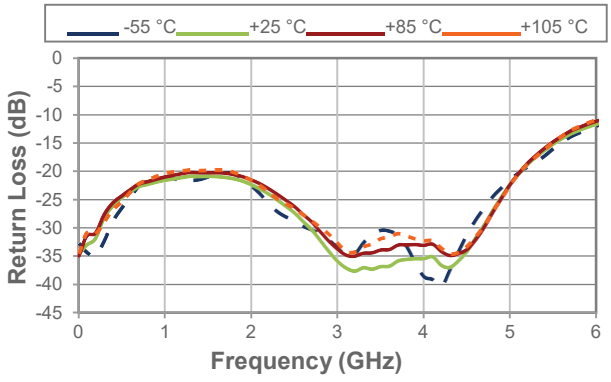



**Figure 5 • *Output Return Loss vs Temp***

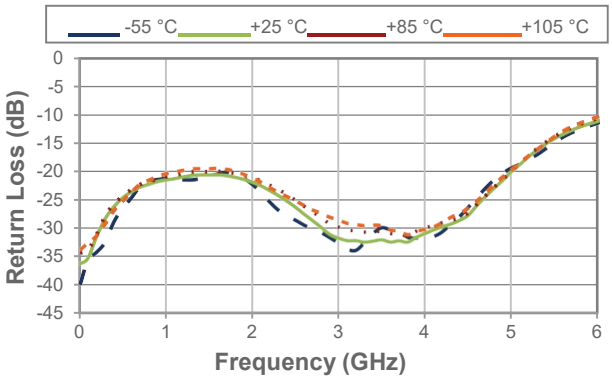


**Figure 6 • $P_{OUT}$ vs $P_{IN}$ Over $V_{CTRL}$ (Limiting Mode @ 915 MHz)**

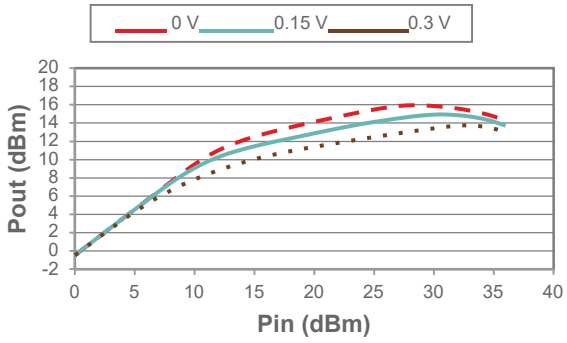



**Figure 7 • $P_{OUT}$ vs $P_{IN}$ Over $V_{CTRL}$ (Limiting Mode @ 6 GHz)**

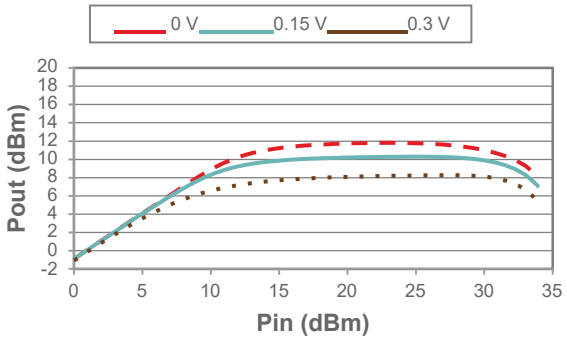



**Figure 8 • P1dB vs $V_{CTRL}$ Over Temp @ 915 MHz**

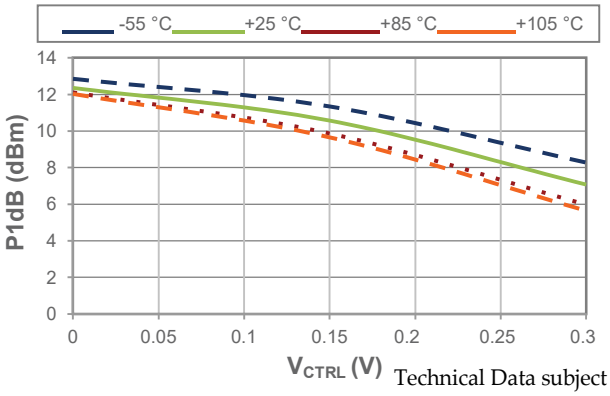



**Figure 9 • $P_{OUT}$ vs $P_{IN}$ Over $V_{CTRL}$ (Reflecting Mode @ 915 MHz)**

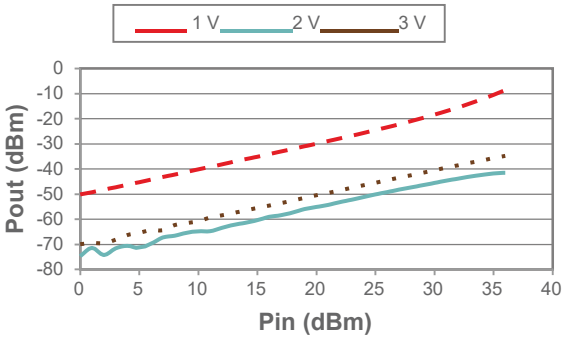



**Figure 10 • $P_{OUT}$ vs $P_{IN}$ Over $V_{CTRL}$ (Reflecting Mode @ 6 GHz)**

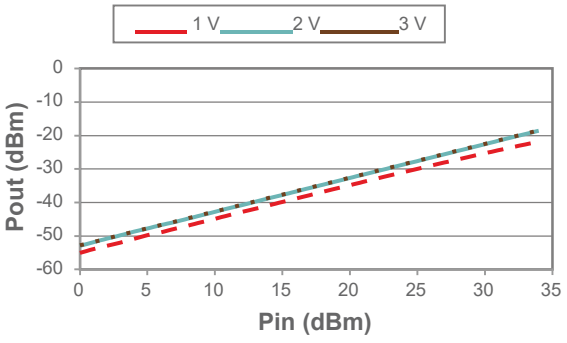



**Figure 11 • P1dB vs $V_{CTRL}$ Over Temp @ 6 GHz**

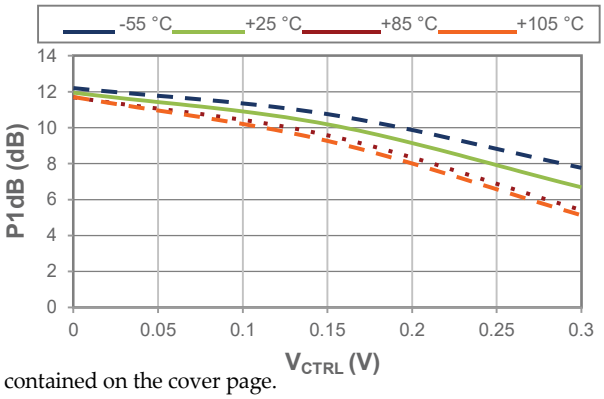


**Figure 12 • *Leakage Power @ $P_{MAX}$ vs $V_{CTRL}$ Over Temp @ 915 MHz***

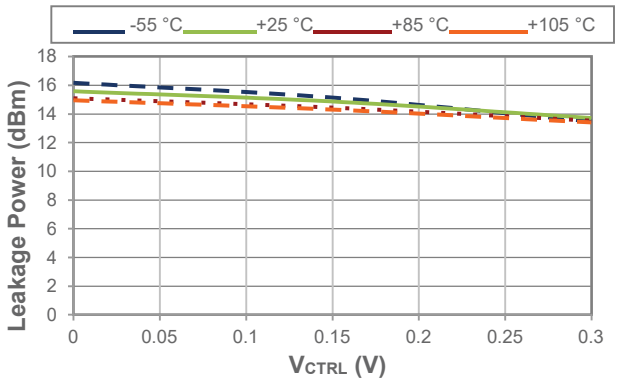



**Figure 13 • *IIP2/IIP3 vs $P_{IN}$ Over $V_{CTRL}$ @ 915 MHz***

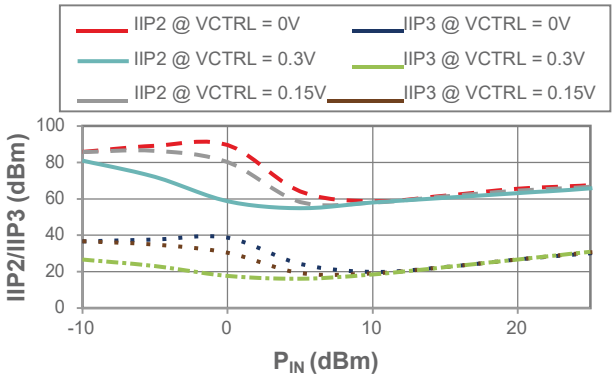



**Figure 14 • *IIP2/IIP3 vs $V_{CTRL}$ Over $P_{IN}$ @ 915 MHz***

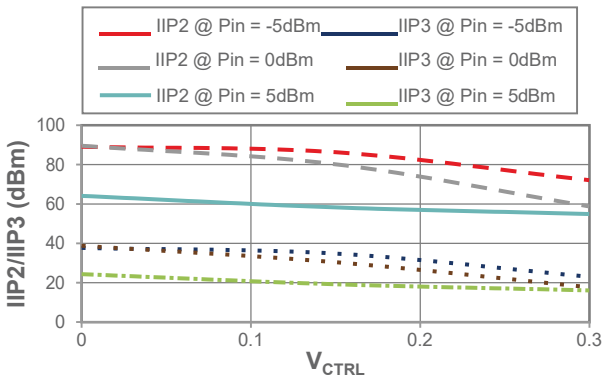



**Figure 15 • *Leakage Power @ $P_{MAX}$ vs $V_{CTRL}$ Over Temp @ 6 GHz***

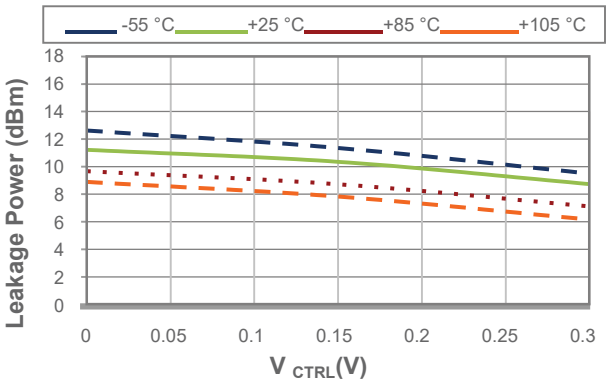



**Figure 16 • *IIP2/IIP3 vs $P_{IN}$ Over $V_{CTRL}$ @ 6 GHz***

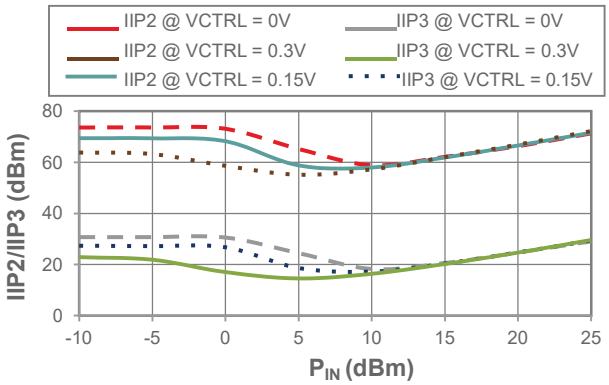
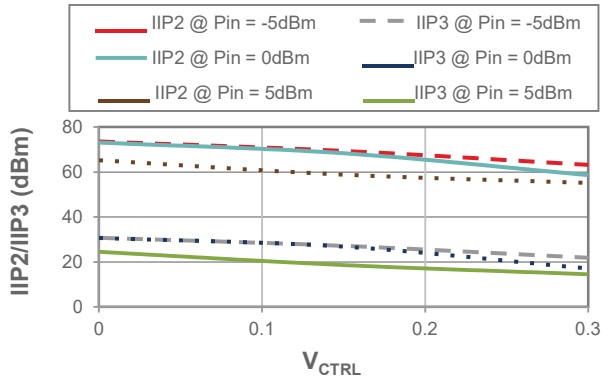



**Figure 17 • *IIP2/IIP3 vs $V_{CTRL}$ Over $P_{IN}$ @ 6 GHz***

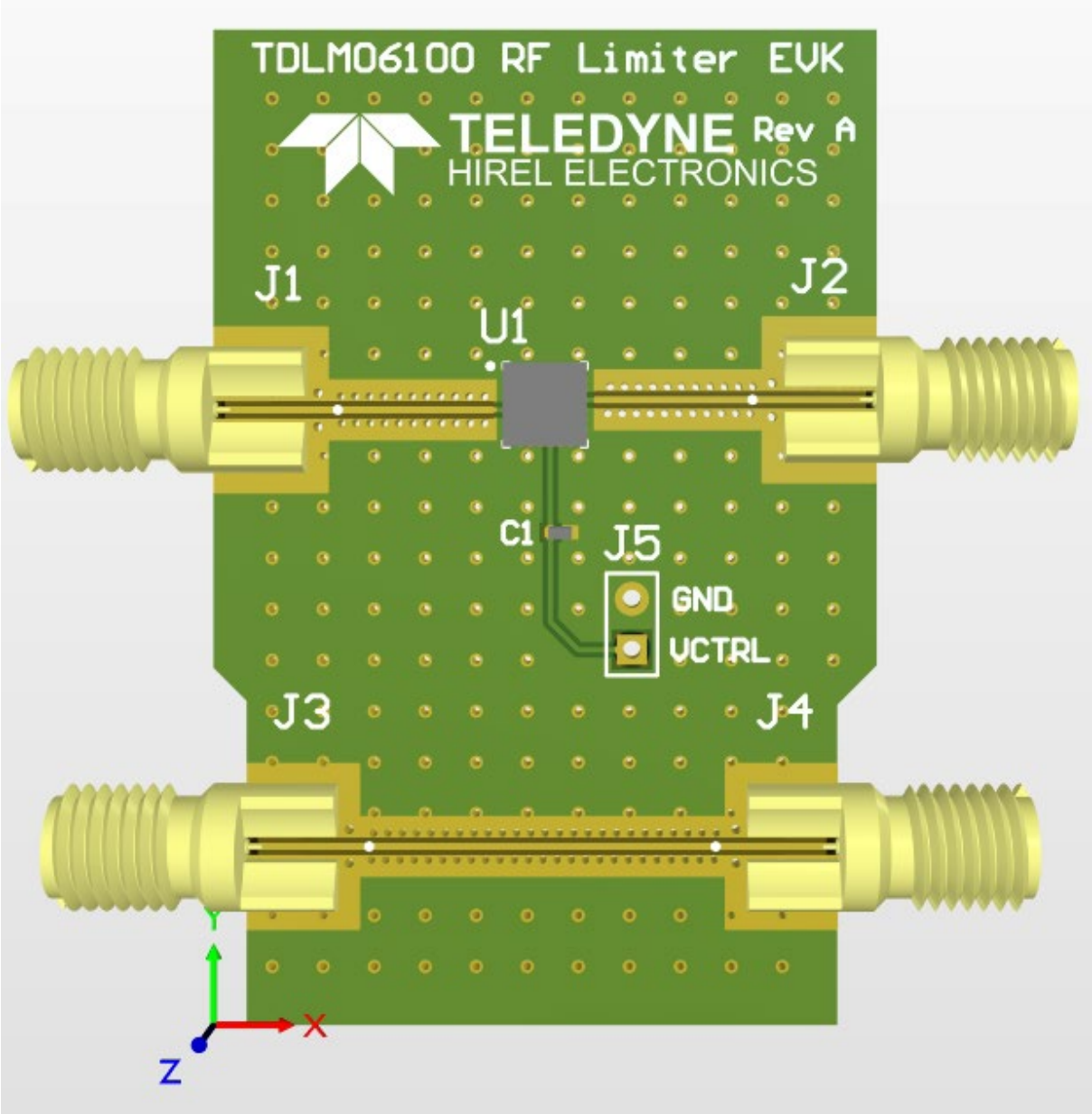


## Evaluation Kit

The power limiter evaluation kit board (EVK) was designed to ease customer evaluation of Teledyne e2v HiRel's TDLM025100. The uni-directional RF input and output are connected to the RF1 and RF2 port through a 50 Ω transmission line via SMA connectors J2 and J3. A through 50 Ω transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connector J4 is connected to the external bias $V_{CTRL}$.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and $\varepsilon_R$ = 3.66. The middle layers provide ground for the trans- mission lines. The transmission lines were designed using a coplanar wavequide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

**Figure 18 • *Evaluation Kit Layout for TDLM025100***



## Pin Information

This section provides pinout information for the TDLM025100. **Figure 19** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

**Figure 19 • *Pin Configuration (Top View)***

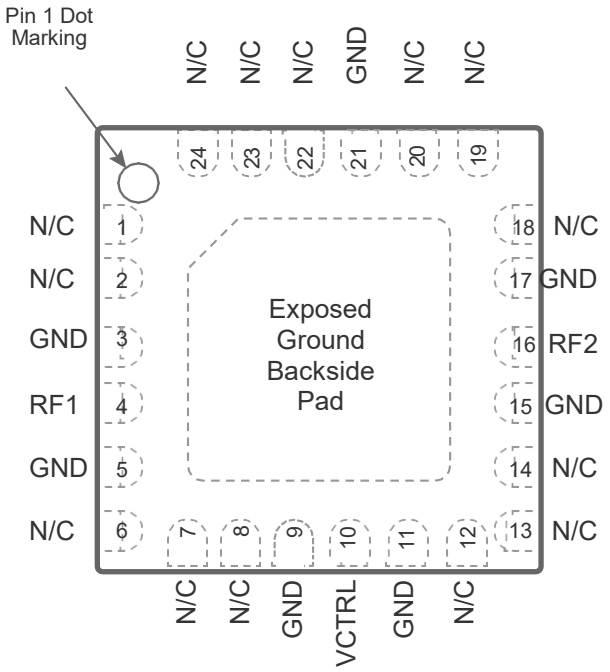



**Table 5 • *Pin Descriptions for TDLM025100***

| Pin No. | Pin Name | Description |
|---|---|---|
| 3, 5, 9, 11, 15, 17, 21 | GND | Ground |
| 4 | RF1(1)(3) | RF port 1 |
| 10 | $V_{CTRL}$ | Control voltage |
| 16 | RF2(1)(3) | RF port 2 |
| 1, 2, 6-8,12-14, 18-20, 22-24 | N/C(2) | No connect |
| Pad | GND | Exposed backside pad: ground for proper operation |

**Notes:**

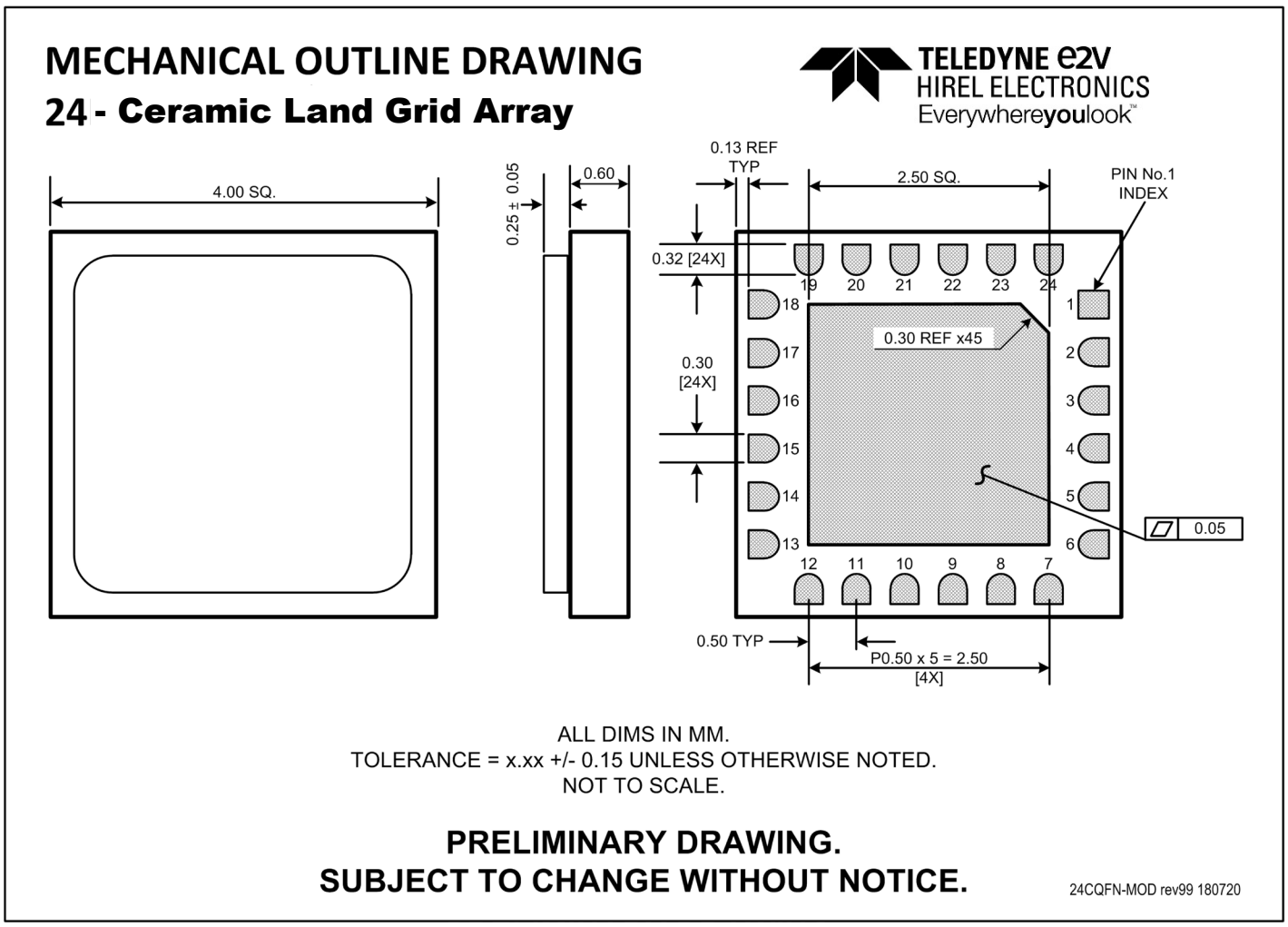
1) RF pins 4 and 16 must be at 0VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0VDC requirement is met.
2) N/C pins can be grounded, if deemed necessary by the customer.
3) The limiter is not bi-directional. RF1 is the RF input and RF2 is the RF output.

# Packaging Information

This section provides packaging data

## Package Drawing

**Figure 20 • *Package Mechanical Drawing for 24-lead 4 × 4 Ceramic LGA***



# Ordering Information

Table 6 lists the available ordering codes for the TDLM025100 as well as available shipping methods.

**Table 6 • *Order Codes for TDLM025100***

| Order Codes | Description | Packaging | Shipping Method |
|---|---|---|---|
| TDLM025100-00 | TDLM025100 Evaluation Kit | Evaluation kit (EVK) | 1/box |
| TDLM025100-01 | TDLM025100 EM Units | 24-lead 4 × 4 Ceramic QFN | Trays |
| TDLM025100–11 | TDLM025100 Flight Units | 24-lead 4 × 4 Ceramic QFN | Trays |



## Document Categories

### Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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